A Wide Dynamic Range CMOS Digital Pixel Sensor

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Abstract - A CMOS image sensor with pixel level analog to digital conversion is presented. Each 13.8µm x 13.8µm pixel area contains a photodiode and a dynamic comparator using the maximum voltage swing available (0V - 1.8V). The comparator does not need any bias current and is insensitive to fabrication process variations. Also a digital to analog converter (DAC) is used to deliver a voltage reference in order to compare it with the pixel voltage for the analog to digital conversion. This DAC provides the possibility to convert the pixel voltage linearly or to compress it logarithmically. The circuit allows image captures at multiple exposure times, and the resulting values are delivered in floating digital format, offering the possibility to expand the intrascene dynamic range to more than 84 dB. The circuit was implemented in a CMOS 0.18µm process and has been submitted for fabrication.

Index Terms - Digital Pixel Sensor, CMOS Image Sensor, Comparator, Analog to Digital Conversion.

I. INTRODUCTION

Charge coupled devices (CCD) technology has been for a long time the technology of choice in high quality image sensing. Drawbacks are high power consumption and no possible on-chip processing capabilities. With CMOS reduced feature size technology, it becomes possible to add on-chip control and processing units in order to obtain a fully integrated camera on a single chip.

On the other hand, as integrated circuit density and speed increase, more and more processing is performed digitally, adding flexibility and eliminating the need for analog tuning. The first CMOS generation of silicon image devices was based on passive pixel sensors (PPS) with analog readout. While those passive sensors suffered from poor signal quality due to the direct transmission of the pixel voltage (integrated charges) on capacitive column busses, CCD based sensors were still preferred for their quality image sensing. With the second generation of image sensors, quality was improved with active pixel sensors (APS), where a buffer transistor (follower) was included in the pixel circuit to prevent destructive readout. The signal read from each pixel was either a current [1] or a voltage [2]. With further increase in circuit speed driven by technology down scaling and reduced supply voltages, precision requirements for pixel analog circuitry became difficult to meet. With reduced feature sizes, more transistors per pixel can be added to the point where a significant part of the pixel circuit is entirely digital. In fact, trends of image sensing are moving towards digital pixel sensors (DPS) that offer numerous advantages such as simplicity, scalability, on-chip processing, low power consumption, wide dynamic range and lower cost. CMOS digital processing can be used to enhance image quality with high intrascene resolution. Nowadays, the demand for portable devices using image sensors rises, driving the need for compact and low power consumption.

In this paper, the dynamic range of CMOS image sensors is addressed. A prototype of a wide dynamic range 32x32 DPS array is presented. The proposed architecture is dedicated to multiple image sampling, high resolution floating point pixel conversion and low power consumption circuit techniques to achieve the requested dynamic range. The remaining parts of this paper include a description of the system architecture in section II. The multiple exposure operation is presented in section III and section IV reports the preliminary results.

II. SYSTEM ARCHITECTURE

A. Image Sensor Array

The architecture of the proposed image sensor is based on novel techniques such as programmable multiple exposure times and user defined pixel transfer function characteristics. This DPS array is intended for wide dynamic range image applications.

The 32x32 pixels image sensor array was implemented to validate the proposed design techniques. Figure 1 shows the block diagram of the system. It includes a pixel array, a one-bit SRAM for each pixel and a cache memory. The one-bit SRAM is used to mark pixels that have reached 50% or more of the full voltage swing in multiple exposure operation (section III). In a normal operation mode, all pixels are reset prior to the integration period. Then after a programmable amount of time, the shutter is closed and the analog to digital conversion is performed by
ramping up the DAC output voltage. The voltage ramp can be linear, logarithmic or any other types. Values of the pixel's intensity are stored sequentially, column by column, in the cache memory.

Figure 1. System components.

The circuit does not need any biasing current, thus when no images are captured (circuit is in idle mode) the sensor array does not consume any power, and there is no need to power up the circuit when a request for a frame capture is received. As a result, no latency is observed between the frame request signal and the sensor response.

B. Pixel Circuit

As shown in Figure 2, the circuit of each pixel contains a photodiode cell, an electronic shutter, a comparator and a lock mechanism to hold the pixel analog's value during multiple exposures operation.

Figure 2. Block diagram of a digital pixel circuit.

The photodiode is based on a N-well/P-substrate structure. During the pixel-reset phase, the photodiode is biased to \( V_{\text{rst}} (V_{\text{th}3.3}+1.8V) \) to maximize the output dynamic range. The photo-generated current decreases the photodiode reverse voltage. During the verification phase, when the array is scanned out, the shutter holds the charges integrated at the gate of the source follower at a constant value. This way, a snapshot of the captured image unaltered during the readout process is obtained. The DPS converts the analog values to a digital format within the pixel. The circuit of each pixel contains a comparator to detect the difference between the integrated charge from the photodiode and an external threshold voltage. This external voltage is generated by a common DAC for the whole DPS array.

The conversion begins while setting the DAC output voltage to 0V and increasing its value monotonically towards \( V_{\text{dd}} \). At each step, the voltage of every pixel \( V_{\text{pix}} \) of the matrix is compared to the DAC generated voltage \( V_{\text{dac}} \). For pixels having \( V_{\text{pix}} \) lower than \( V_{\text{dac}} \), the corresponding digital DAC value is stored in the cache memory.

It is important to note that maintaining needed analog processing within each pixel reduces the overall system power consumption [3]. Figure 3 illustrates the compact 13.8µm square pixel layout with a fill factor of 29%, including the circuitry for analog to digital conversion.

Figure 3. Pixel layout.

The CMOS 0.18µm process allows circuits that can be based on two power supplies, 1.8V and 3.3V. Generally, 1.8V is used for the core circuit, however 3.3V is used to power up the I/O pads. Nevertheless, it is possible to power the core circuit with 3.3V at the cost of using larger transistors. Benefits from using 0.18µm technology to design reduced size image sensors require small dimensions transistors, hence 1.8V transistors are used for the pixel comparator circuit. With a NMOS transistor follower (Figure 4), inputs \( V_{\text{photo}} \) below the device threshold voltage are not efficient. Since, this design intends to exploit the maximum dynamic range of 1.8V transistors, a large transistor supporting voltages up to 3.3V for the follower is employed. In this case, a reference voltage \( V_{\text{rst}} \) higher than 1.8V is applied to the follower's input in order to get the maximum output voltage swing at its source \( V_{\text{pix}} \).

Figure 4. Shutter/Follower circuit.

C. Comparator

Special care has been paid to build a small area comparator intended to fit within each pixel circuit. The proposed comparator must operate at the highest voltage swing with
a reduced offset voltage to achieve the highest possible precision. The design of a mismatch insensitive comparator using the same path for both compared inputs reduces its offset voltage.

Figure 5 presents the schematic diagram of the comparator. Switched capacitors circuit is used to perform the comparison. The capacitor, using two metal layers, is built on top of the pixel to minimize its area. This technique allows to protect the circuitry from photo-induced currents. Also, the comparator circuit uses the full voltage dynamic range (0V-1.8V).

Three clock phases are used to perform a comparison, \( \Phi_1 \), \( \Phi_2 \) and validate. The validate phase gives a valid output for very small difference between the inputs. From the charge conservation law given in equation (1), expression (2) gives the voltage across the capacitor during charge conservation law given in equation (1), expression (3). \( V_{\text{pix}} \) is the input difference amplified by inverter A1 (centered to \( V_{\text{dd}/2} \)). When \( \Phi_2 \) is active (3), \( V_a \) is set to the comparison threshold \( V_{\text{dd}} \) and \( V_b \) is equal to \( V_{\text{dd}/2} \) plus the difference between the inputs, leading to equation (4) from (2) and (3). \( V_b \) is then amplified by inverter A1 (centered to \( V_{\text{dd}/2} \)) to give \( V_c \), and amplified a second time by inverter A2 to give \( V_{\text{comp}} \) that is set to the input difference amplified by the two inverter gains (5).

\[
Q = C(V_a - V_b) \quad \text{(1)}
\]
\[
Q = C(V_{\text{pix}} - V_{\text{dd}/2}) \quad @ \, \Phi_1 \quad \text{(2)}
\]
\[
Q = C(V_{\text{dd}} - V_b) \quad @ \, \Phi_2 \quad \text{(3)}
\]

\[
V_b = (V_{\text{dd}} - V_{\text{dd}/2}) + V_{\text{dd}/2} \quad \text{(4)}
\]
\[
V_{\text{comp}} = A_1A_2(V_{\text{dd}} - V_{\text{pix}}) + V_{\text{dd}/2} \quad \text{(5)}
\]

If this voltage difference \( V_{\text{pix}} - V_{\text{dd}} \) is too small to give a valid digital output (0V or \( V_{\text{dd}} = 1.8 \text{V} \)), a validate signal that activates a positive feedback loop (6) is generated in order to saturate the output quickly.

\[
V_b = V_{\text{comp}} \quad @ \, \text{validate} \quad \text{(6)}
\]

III. MULTIPLE EXPOSURES OPERATION

The proposed architecture is primarily intended for multiple exposures operation with a shutter lock feature. In multiple sampling mode, image capture starts with the photodiode matrix reset, then the voltage integration at the gate of the follower begins. After a programmable period of time (T), a verification is performed to identify the pixels that have reached 50% of the full voltage dynamic range. Those pixels are marked in the 1-bit SRAM, the time tag (TG) is stored in the cache memory and their shutter are locked until the next image reset. The integration goes on until the next verification is performed at the following programmed time, which is usually at 2T, 4T, ..., 2kT, in order to achieve floating point resolution [4]. For the last exposure, all pixel values are converted, as explained in section II, and stored with the time tag in the cache memory. Also, this multiple exposures approach allow to achieve higher signal-to-noise ratio [6].

Figure 6 illustrates the multiple exposures operation for four pixels. Each pixel receive a different light illumination. At the first verification time (T), the brighter pixel (a) has a greater than \( V_{\text{dd}/2} \) value, so it is marked in the SRAM and the TG value (00) is stored in the cache memory. At the following verification times 2T, 4T and 8T, pixels (b), (c) and (d) are marked respectively and then the A/D conversion is performed. Pixel (a) final digital value is 1872, given by equation (7), which is a floating point representation. Table I lists the other pixel values.

\[
R = V_{\text{pix}}2^{(T_{\text{max}} - TG)} \quad \text{(7)}
\]

Table I. Cache memory values for pixels shown in Figure 6

<table>
<thead>
<tr>
<th>Pixel</th>
<th>SRAM/TG</th>
<th>DAC</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( T )</td>
<td>( 2T )</td>
<td>( 4T )</td>
</tr>
<tr>
<td>a)</td>
<td>0/XX</td>
<td>0/XX</td>
<td>0/XX</td>
</tr>
<tr>
<td>b)</td>
<td>0/XX</td>
<td>1/00</td>
<td>1/00</td>
</tr>
<tr>
<td>c)</td>
<td>0/XX</td>
<td>0/XX</td>
<td>0/XX</td>
</tr>
<tr>
<td>d)</td>
<td>0/XX</td>
<td>0/XX</td>
<td>0/XX</td>
</tr>
</tbody>
</table>

IV. PRELIMINARY RESULTS

The intrascene dynamic range of an image depends on the minimum and maximum exposure time which depends on
the transfer rate and the dark current, respectively. With an array of 320x320 (10 times more rows and columns than the prototype array), and with a system clock of 50 MHz, the minimum exposure time is 6.4µs (320 columns / 50 MHz). The maximum exposure time depends on the dark current of 27.65fA calculated from [5] (diode surface of 55.31µm² and typical leakage of 50nA/cm²). With this value, a voltage span from \( V_{di} \) (2.7V) to \( V_{photoMin} \) (0.3V) quantified in 256 levels (8-bit) and the photodiode capacitance of 1.53fF, the resulting maximum integration time is 519µs (\( v = it \)). With a minimum and maximum exposure time of \( T = 6.4\mu s \) and \( 2^N \) respectively, the resulting N is 6 (\( 2^N = 64 \)). The calculated dynamic range, with 8 bits quantification for the mantissa and 6 exponentially increasing extra exposure times, is \( 20\log(2^{8\times6}) = 84\text{dB} \).

The locking shutter allows for wide dynamic range imaging with low volume off chip data transfer. In fact, to achieve wide dynamic range resolution, most of the existing sensors acquire multiple pictures using different exposures and then, off-chip processing is done to recombine them in one image [4]. In such architecture, pixel values need to be transferred as many times as there are different exposure times, giving an amount of data transferred per image equal to \( RCBE \text{ Rows, Columns, Bits/pixel, different Exposures} \). However, the proposed architecture only necessitates \( RC(B+E) \). Hence, the data transfer for typical values of 8 for B and E is reduced by a factor of 5.8, as shown by equation (8).

\[
\eta = \frac{BE}{B+\log_2 E}
\]  

(8)

Although, \( \eta \), could be higher for larger values of B and E. Another advantage of the proposed multiple exposures architecture is that there is no need to post-process the data to obtain the final wide dynamic range single image. This feature contributes to lower the overall system power. For applications where the frame rate is very low, surveillance camera or digital still photography, the system can power down very easily between each image capture resulting in very low power consumption.

The spectre simulation under Cadence environment using CMOS 0.18µm technology allows to confirm the expected characteristics as shown in Table II. Also, the simulation of the implemented layout that is currently under fabrication by Taiwan Semiconductor Microelectronic Corporation (TSMC), confirmed the suited operation. Since we do not have the chip to measure the fixed pattern noise FPN and power consumption accurately and simulation does not provide valuable results, those parameter values are not presented in Table II, but will be available as soon as the chip is received.

### Table II. DPS Chip Summary.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18µm Nwell CMOS</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>3.3V and 1.8V</td>
</tr>
<tr>
<td>Package</td>
<td>84 pin PGA</td>
</tr>
<tr>
<td>Array Size</td>
<td>32x32 pixels</td>
</tr>
<tr>
<td>Photodector type</td>
<td>Photodiode</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>13.8µm x 13.8µm</td>
</tr>
<tr>
<td>Fill Factor</td>
<td>29%</td>
</tr>
<tr>
<td>Transistor / pixel</td>
<td>26</td>
</tr>
<tr>
<td>Dynamic Range*</td>
<td>84dB</td>
</tr>
</tbody>
</table>

* Obtained by numerical calculation

\[ V_{di} = 2.7V \]
\[ V_{photoMin} = 0.3V \]
\[ C = 1.53fF \]
\[ T = 6.4\mu s \]
\[ N = 6 \]

V. CONCLUSION

A wide dynamic range image sensor with pixel level ADC was described. The design of the 13.8µm x 13.8µm digital pixel has been possible with the use of a small area, high resolution and mismatch insensitive comparator. The pixel contains a photodiode circuit, a comparator and a shutter. Simulations have proven the suited functionality for image captures using multiple exposure times and image reconstitution with low power reduced data transfer. The test chip is currently in fabrication and experimental results are expected in the near future.

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REFERENCES